Muhammad Hadir Khan

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EDUCATION

Ph.D. in Computer Science and Engineering *Started* Sep, 2021
University of California, Santa Cruz

B.E in Electrical Engineering, 2019
NED University of Engineering and Technology *Karachi, Pakistan*

INDUSTRY EXPERIENCE

Luminous Computing Austin, U.S June, 2022 – Sep, 2022

CPU Engineering Intern

- Worked on Very Long Instruction Word (VLIW) hardware accelerator and added vector instructions to speed up certain Machine Learning (ML) algorithms.
- Worked on porting a part of the accelerator on Field Programmable Gate Arrays (FPGAs) to analyze performance gains and rough area estimate.

RESEARCH EXPERIENCE

VLSI Design and Automation Group Santa Cruz, U.S Sep, 2021 – Present

Graduate Student Researcher

- Created a wishbone bus interface and memory map in Verilog to test more OpenRAM generated SRAMS and submitted the design in the Efabless Open MPW Shuttle Program by Google. (https://github.com/VLSIDA/openram_testchip)

Micro-Electronics Research Laboratory Karachi, Pakistan Aug, 2019 – Aug, 2021

Research Associate *Aug, 2020 – Aug, 2021*

- Designed a 5 stage pipelined RV32IM CPU in CHISEL and emulated the core on an FGPA successfully running C programs. (https://github.com/hadirkhan10/Buraq-mini)
- Designed the TileLink Uncached Lightweight (TL-UL) protocol in CHISEL. (https://github.com/hadirkhan10/TileLink)
- Designed a System on a Chip (SoC) around the core with memories and peripherals (UART, GPIO) which was selected for the first fully open-source tape-out through the Efabless Open MPW Shuttle Program by Google on a 130nm process from Skywater PDK. (github.com/hadirkhan10/caravel_ibtida_soc.git)

Research Assistant Aug, 2019 – Aug, 2020

- Gained familiarity with the RISC-V ISA and its Assembly, GNU Toolchain and C programming.
- Gained familiarity with FPGAs, Verilog, SystemVerilog and CHISEL.
- Designed a single cycle CPU with CHISEL and emulated the core on the Arty-A7 FPGA. (https://github.com/hadirkhan10/Single-Cycle-CPU)

SKILLS, LANGUAGES, AND TOOLS

- Python
- Assembly programming
- Hardware generation with CHISEL
- Embedded programming
- Hardware design with Verilog
- iverilog
- Verilator
- GTKWave
- Magic VLSI tool
- IRSIM
- netgen
- OpenLane

PUBLICATIONS

- H. Khan, "How Chisel is making designing processors interesting for Software Engineers", 2020. Available at: https://medium.com/@hadirkhan10/how-chisel-is-making-designing-processors-interesting-for-software-engineers-88a84492cfc8
- Khan, Muhammad Hadir; Jalal, Aireen Amir; Ahmed, Sajjad; Ansari, Ali Ahmed; Naqvi, Syed Roomi (2021): IBTIDA: Fully open-source ASIC implementation of Chisel-generated System on a Chip. TechRxiv. Preprint. https://doi.org/10.36227/techrxiv.16663738.v1

TRAININGS

Instructor – Short Open Course on Digital Design with Chisel

- Mentored undergraduate students to design their own RISC-V processors in CHISEL. (https://github.com/merledu/Markhor-Core)

WEBINARS AND WORKSHOPS

- "An Open Source Microprocessor Designing Initiative in Pakistan" at Habib University. (https://youtu.be/5PV5bYw8-Os?t=1350)
- "RISC-V Based core in Chisel and Emulation on FPGA: An Open Source Microprocessor Designing Initiative in Pakistan" at IEEE NED Computer Society. (https://youtu.be/n1WnXPTwFfU?t=3810)

ACADEMIC HONORS

- Dean's fellowship, UC Santa Cruz
- Department fellowship, UC Santa Cruz
- Hajiani Amina Hasham Meritorious Scholarship, UIT
- Gold Medal, Merit Certificate and Cash award, UIT